

REMARKS

Claims 8-14 are presently pending and stand rejected. Claims 1-7 are cancelled without prejudice.

Claims 8-14 were rejected under 35 U.S.C. 101 for being "without any article or physical transformation, result, or produce any useful concrete tangible result." Office Action, at 2.

Assignee respectfully traverses the rejection and notes that claim 8 recites, among other limitations, "a first memory", which is an article. For this reason alone, the rejection to claim 8 and dependent claims 9-14 under 35 U.S.C. 101 should be withdrawn.

Additionally, claim 8 recites, among other limitations, "displaying frames" which is a concrete tangible result. For this reason alone, the rejection to claim 8 and dependent claims 9-14 under 35 U.S.C. 101 should be withdrawn.

Additionally, claim 8 recites, among other limitations, "a first memory for storing a top field". It is respectfully submitted that when the memory stores the top field, it is physically transformed either, electrically, electromagnetically, and/or chemically. For this reason alone, the rejection to claim 8 and dependent claims 9-14 under 35 U.S.C. 101 should be withdrawn.

Claims 8-14 were rejected under 35 U.S.C. 102(b) as anticipated by Jun, U.S. Patent 6,040,868.

Claim 8 recites, among other limitations, "a first memory for storing a top field" and "a second memory for storing a bottom field, the bottom field being associated with the top field".

Examiner has indicated that in Jun, "The memories 10 and 20 each stores a respective video field, such as the

even and odd fields, which are the same as the top field and the bottom field as claimed." Office Action, 1-2. Examiner has also indicated that "Jun shows a first memory (50), a second memory (60-90), ... in Figure 4." Office Action, at 2.

Assignee calls Examiner's attention to Jun, Col. 4, Lines 2-4, "first and second memories 10 and 20 each for storing the scanning line signals corresponding to a horizontal period,". In contrast, claim 8 recites "a first memory for storing a top field" and "a second memory for storing a bottom field, the bottom field being associated with the top field". Assignee respectfully submits that "a top field" and a "bottom field" does not read on the "line signals corresponding to a horizontal period" taught by Jun. In Jun, Figure 4, reference numerals 50 and 60-90 merely refer to "line memory". Again, Assignee respectfully submits that "a first memory for storing a top field" and "a second memory for storing a bottom field" do not read on the "line memory" taught by Jun. Accordingly, Assignee for this reason alone, traverse the rejection to claim 8, and dependent claims 9-14, and requests that Examiner withdraw it.

Claim 8 recites, among other limitations, "a feeder for fetching a first line from the top field, fetching a first line from a bottom field corresponding to the top field after fetching the first line from the top field, and fetching a second line from the top field after fetching the first line from the bottom field, the second line from the top field being adjacent to the first line in the top field".

Examiner has indicated that in Jun "the line memories 50-90, read clock generator 170, R/W clock generator and

multiplexer 100 and 120 together meet the fetching steps as claimed." Examiner has also made reference to Jun, Figure 2, SW4, and Figure 4, 100, 200.

Assignee calls Examiner's attention to Jun, col. 4, lines 57-60, where "Fig. 4 which illustrates a video display converting circuit for converting scanning patterns from interlaced scanning to sequential scanning". Similarly Jun, Col. 4, Line 57-60 also "illustrates a video display converting circuit for converting scanning patterns from interlaced scanning to sequential scanning". In an interlaced scan, "a first field having 'even' lines is scanned. At this point, the beam starts downward to scan a second field as before, and the second field has '[t]odd' r lines that are interlaced with the 'even' lines of the first field."

Thus, multiplexer 100, 120 would not be "fetching a first line from the top field, fetching a first line from a bottom field corresponding to the top field after fetching the first line from the top field, and fetching a second line from the top field after fetching the first line from the bottom field, the second line from the top field being adjacent to the first line in the top field".

Accordingly, for the foregoing reason alone, Assignee respectfully traverse the rejection to claim 8 and dependent claims 9-14, and requests that Examiner withdraw it.

Claim 9 recites, among other limitations "a line address computer for calculating a starting address for a row of luma pixels and calculating a starting address for a row of chroma pixels". Examiner has indicated that "the write clock generator 30 and read clock generator 40 meets the calculating steps as claimed because they both

generates address signals to the memories 10 and 20."

Assignee respectfully disagrees with Examiner's characterization of Jun, that "write clock generator 30" and "read clock generator 40" "generate address signals to the memories 10 and 20." While Jun states that "write clock signal is alternatively supplied to each of the first and second memories 10 and 20 during every other horizontal period as shown in Fig. 3B" and that "During the alternating horizontal period, the read clock signal is supplied to the other one of memories 10 and 20", the foregoing does not teach generating an "address", or "address signal", much less "calculating a starting address for a row of luma pixels and calculating a starting address for a row of chroma pixels". Accordingly, Assignee respectfully traverse the rejection to claim 9 and dependent claims 10-14, and requests that Examiner withdraw it.

The Commissioner is hereby authorized to charge additional fees or credit overpayments to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

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Respectfully submitted,



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